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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,173	08/30/2004	Rebecca S. Taylor	6057-30702	5172

35690 7590 04/07/2009

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EXAMINER	
TRAN, BANGLONG	

ART UNIT	PAPER NUMBER
2458	

MAIL DATE	DELIVERY MODE
04/07/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/711,173	Applicant(s) TAYLOR, REBECCA S.	
	Examiner BANGLONG TRAN	Art Unit 2458	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 30 August 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 August 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12/11/2006; 05/05/2008.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 are now pending in this application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 2, 7, 8, 12-19, 26-30 and 31-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claims 1, 2, 7, and 8 are not limited to tangible embodiments. These claims recited "A generic protocol translator that translates information from a source device to a destination device, comprising: a receiver circuit manager..., one or more receivers..., a message router...." are just limited to a functional descriptive materials consisting of computer program per se ([0153], line 3-6, receiver circuit manager further comprises one or more interface socket, i.e., interface socket could be a program), instead of being defined as including tangible embodiments (i.e., a computer readable storage medium such as memory device, storage medium, etc.,), As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

5. Claim 12 is a method claim but not tied to any particular machine or transform underlying subject matter (such as an article or material) to a different state or thing. Therefore, the claimed invention is directed to non-statutory subject mater.

Claims 13-19 are depending on claim 12 and therefore also rejected as claim 12 above.

6. Claim 26 is an apparatus claim and rejected under 35 U.S.C. 101 because the claim recited "a logic unit...." is just limited to a functional descriptive material consisting of software per se instead of being defined as including tangible embodiments (i.e., a computer readable storage medium such as memory device, storage medium, etc.,), As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claims 27-30 are depending upon claim 26 and therefore also rejected as claim 26 above.

7. Claim 31 is an apparatus claim and also rejected under 35 U.S.C. 101 because the claim recited “an input/output unit…first mean for…” is just limited to a functional descriptive material consisting of software per se ([0040], lines 3-5, the WAP gateway 22, i.e., WAP gateway 22 means input/out put unit and is configured to communicate to the external devices as interpreted by The Examiner) instead of being defined as including tangible embodiments (i.e., a computer readable storage medium such as memory device, storage medium, etc.,), As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claims 32-33 are depending upon claim 31 and therefore also rejected as claim 31 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey et al. (hereinafter Dorsey), U.S Patent No. 6198751, in view of Broulik et al. (hereinafter Broulik), U. S Patent No.6323881.

10. As to claim 1, Dorsey discloses a generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4. line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives information from a source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 5, lines 28-30; column 6, lines 10-11, i.e., the network interface 20a embedded in a networking device configured to received packets from a network and packets got translated by multi-protocol translator 26 and direct memory access controller 27 and then packets are forwarded to network interface 20b embedded in another networking device meaning receiver circuit manager receives information from a source device that is intended for a destination device through said interface sockets);

one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4, lines 20-22).

Dorsey does not disclose

a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey with the teaching of Broulik to have a message router that determines which destination protocol is appropriate for the

information. Because it would provide users a better method to avoid full-feature TCP handling on the proxy but still achieve live protocol translation at line-speed in a TCP–compliant, TCP-friendly manner, translate a protocol connection request to another protocol connection type when receiving a protocol connection request to a particular destination address or host name.

11. As to claim 2, Dorsey discloses a system with a generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives information from a source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 6, lines 10-11);

one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to

support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

The motivation of this claim is as same as the one of claim 1 above.

12. As to claim 3, Dorsey discloses a method to make generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

providing a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives

information from a source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 6, lines 10-11);

providing one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

providing one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

providing one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

providing a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

providing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

The motivation of this claim is as same as the one of claim 1 above.

13. As to claim 4, Dorsey discloses a method that translates information from a source device to a destination device using a generic protocol translator (Fig.2, translator 28, column 4, lines 15-20), comprising:

receiving information with a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) from a source device where the information is intended for a destination device (column 4, lines 20-22; column 6, lines 10-11), said receiver circuit manager further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3);

receiving information with one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

converting information with one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

sending information with one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

routing information with a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

routing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

The motivation of this claim is as same as the one of claim 1 above.

14. As to claim 5, Dorsey discloses a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform a method that translates information from a source device to a destination device using a generic protocol translator (Fig.2, translator 28, column 4, lines 15-20), comprising:

receiving information with a receiver circuit manager from a source device where the information is intended for a destination device, said receiver circuit manager further comprises one or more interface sockets, each interface socket is assigned a supported source protocol,

receiving information with a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) from a source device where the information is intended for a

destination device (column 4, lines 20-22; column 6, lines 10-11), said receiver circuit manager further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3);

receiving information with one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

converting information with one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

sending information with one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

routing information with a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

routing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

The motivation of this claim is as same as the one of claim 1 above.

15. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Broulik as applied to claim 5 above, in view of Nackman et al. (hereinafter Nackman), U.S Patent No. 4797842, and further in view of Sternberg et al. (hereinafter Sternberg), U.S Patent No. 4290049.

16. As to claim 6, Dorsey and Broulik disclose the invention as described in claim 5 above, Dorsey and Broulik do not disclose the conversion process uses a poly dimensional finite state automaton that further comprises a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix

wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Broulik and Nackman with the teaching of Sternberg to have the conversion process uses a poly dimensional finite state automaton that further comprises a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage. Because it would provide users a better method to completely automate so that no interactive assistance is required from user, minimize processing times and the cost of implementation of hardware when analyzing complex images.

17. As to claim 7, Dorsey discloses a generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives information from a source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 6, lines 10-11);

one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65) and can be reprogrammed in the field to support other protocols (column 4, lines 7-14), device types (column 4, lines 41-44), and applications (column 6, lines 65-67);

one or more message senders (Fig.2, network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4, lines 20-22).

Dorsey does not disclose

a message router that determines which destination protocol is appropriate for the information; and

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Broulik discloses

a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

Dorsey and Broulik do not disclose

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

The motivation of this claim is as same as the ones of claim 1 and 6 above.

18. As to claim 8, Dorsey discloses a system with a generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives information from a

source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 6, lines 10-11);

one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65) and can be reprogrammed in the field to support other protocols (column 4, lines 7-14), device types (column 4, lines 41-44), and applications (column 6, lines 65-67);

one or more message senders (Fig.2, network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4, lines 20-22).

Dorsey does not disclose

a message router that determines which destination protocol is appropriate for the information; and

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein

one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Broulik discloses

a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

Dorsey and Broulik do not disclose

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

The motivation of this claim is as same as the ones of claim 1 and 6 above.

19. As to claim 9, Dorsey discloses a method to make generic protocol translator that translates information from a source device to a destination device (Fig.2, translator 28, column 4, lines 15-20), comprising:

providing a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) that further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3), said receiver circuit manager receives information from a source device that is intended for a destination device through said interface sockets (column 4, lines 20-22; column 6, lines 10-11);

providing one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

providing one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that

uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

providing one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

providing a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

providing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

Dorsey and Broulik do not disclose

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

The motivation of this claim is as same as the ones of claim 1 and 6 above.

20. As to claim 10, Dorsey discloses a method that translates information from a source device to a destination device using a generic protocol translator (Fig.2, translator 28, column 4, lines 15-20), comprising:

receiving information with a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) from a source device where the information is intended for a

destination device (column 4, lines 20-22; column 6, lines 10-11), said receiver circuit manager further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3);

receiving information with one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

converting information with one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

sending information with one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

routing information with a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

routing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

Dorsey and Broulik do not disclose

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is

obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

The motivation of this claim is as same as the ones of claim 1 and 6 above.

21. As to claim 11, Dorsey discloses a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform a method that translates information from a source device to a destination device using a generic protocol translator (Fig.2, translator 28, column 4, lines 15-20), comprising:

receiving information with a receiver circuit manager from a source device where the information is intended for a destination device, said receiver circuit manager further comprises one or more interface sockets, each interface socket is assigned a supported source protocol,

receiving information with a receiver circuit manager (Fig.2, network interface 20a, column 4, lines 20-22) from a source device where the information is intended for a destination device (column 4, lines 20-22; column 6, lines 10-11), said receiver circuit manager further comprises one or more interface sockets (Fig.2, the header 22a, column 4, line 67), each interface socket is assigned a supported source protocol (column 4, lines 64-67; column 5, lines 1-3);

receiving information with one or more receivers (Fig.2, input memory 21a, column 4, lines 45-51) that receive information from said receiver circuit manager (column 5, lines 18-19; column 7, lines 18-21);

converting information with one or more message converters (Fig.2, multi-protocol translator 26, direct memory access 27) that convert the information to the destination format that uses a conversion process (column 5, lines 22-25), said message converters are extensible (column 6, line 65, flexible means extensible) and can be reprogrammed in the field to support other applications (column 6, lines 65-67), protocols (column 4, lines 7-14), device types (column 4, lines 41-44, i.e., payload means message body implied device types as cited in the specification of instant application);

sending information with one or more message senders (Fig.2 network interface 20b) that transfer the information in the destination format and protocol to the destination device (column 4. lines 20-22).

Dorsey does not disclose

routing information with a message router that determines which destination protocol is appropriate for the information;

However, Broulik discloses

routing a message router (Fig.2, proxy 26) that determines which destination protocol is appropriate for the information (column 4, lines 32-39).

Dorsey and Broulik do not disclose

the conversion process uses a poly dimensional finite state automaton that further comprises a multi-stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage

However, Nackman discloses

the conversion process uses a poly dimensional finite state automaton (column 9, lines 4-7),

Dorsey, Broulik and Nackman do not disclose

a multi stage pipeline comprising a first stage and a plurality of subsequent stages, wherein each stage of said multi-stage pipeline further comprises a matrix wherein a result is obtained as a function of one or more input variables, wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage.

However, Sternberg discloses

a multi stage pipeline (column 3, lines 53-54) comprising a first stage and a plurality of subsequent stages (column 3, lines 54-55) wherein each stage of said multi-stage pipeline further comprises a matrix (column 3, lines 59-62) wherein a result is obtained as a function of one or more input variables (column 4. lines 37-42), wherein one of said input variables of each said subsequent stage further comprises the result from a prior stage (column 4, lines 3-4).

The motivation of this claim is as same as the ones of claim 1 and 6 above.

22. Claims 12-14, 19, 20, 26, 30-32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Nackman, in view of Sternberg.

23. As to claim 12, Dorsey discloses a method, comprising:

receiving an input message transmitted using a source communication protocol (column 4, lines 20-22; 64-66, i.e., source address can be used to determine source protocol meaning input message transmitted using a source communication protocol), wherein the input message has a source data format (column 12, lines 8-12, 2-bytes of information from the data packet);

generating an output message from the received input message (column 5, lines 25-27, i.e., translating the header and trailer information from the first protocol in to the header and trailer information for the new packet meaning generating an output message), wherein the output message has a destination data format (column 5, lines 25-27, i.e., the header and trailer information for the new packet meaning a destination data format) and is to be transmitted using a destination communication protocol (column 5, lines 28-30, i.e., transmission across the second network meaning transmitted using a destination communication protocol);

convert the source communication protocol of the input message to the destination communication protocol of the output message (column 9, line 55-61); and

convert the source data format to the destination data format of the output message (column 10, lines 2-3);

inputs indicative of the source data format (column 12, lines 8-12), the source communication protocol (column 9, lines 55-61), the destination data format (column 10, lines 2-3; column 12, lines 8-12, source and destination data have the same format), and the destination communication protocol (column 9, lines 55-61).

Dorsey does not disclose

the generating includes using a multi-stage, multi dimensional finite state machine.

However, Nackman discloses the generating includes a multi dimensional finite state machine (column 9, lines 4-7).

Dorsey and Nackman do not disclose

the generating includes using a multi-stage machine.

However, Sternberg discloses

the generating includes using a multi-stage machine (column 3, lines 53-54).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Nackman with the teaching of Sternberg to have the generating includes using a multi-stage, multi dimensional finite state machine. Because it would provide users a better method to avoid full-feature TCP handling on the proxy but still achieve live protocol translation at line-speed in a TCP–compliant, TCP-friendly manner, translate a protocol connection request to another protocol connection type when receiving a protocol connection request to a particular

destination address or host name, to completely automate so that no interactive assistance is required from user, minimize processing times and the cost of implementation of hardware when analyzing complex images.

24. As to claim 13, Sternberg discloses the finite state machine having a first stage and one or more additional stages (column 3, lines 53-55, i.e., a plurality of serially connected stages implying a first stage), wherein each of the stages generates an output from two or more inputs to that stage (column 7, lines 40-43) using a multidimensional matrix (column 17, lines 55-57), and wherein each of the one or more additional stages includes the previous stage's output as an input (column 4, lines 3-4).

25. As to claim 14, Dorsey discloses determining, from the input message, the source communication protocol (column 9, lines 55-56) and source data format (column 12, lines 8-12).

26. As to claim 19, Dorsey discloses sending the output message to a second device using the destination data format and the destination communication protocol, both of which are supported by the second device (column 5, lines 29-31, i.e., interface 20b meaning second device, it would have been obvious to the one skilled in the art to recognize the destination data format and destination protocol when the package translation is finished).

20. As to claim 20, Dorsey discloses an apparatus, comprising:

one or more processors (Fig.2, multi-protocol translator 26, direct memory access controller 27, column 5, line 23-25);

a memory (Fig.2, memory 21a, column 4, lines 46-51) storing program instructions executable by the one or more processors to:

receive an input message (column 5, lines 7-9); and

perform data format conversion and protocol conversion of the input message to generate an output message (column 5, lines 23-27)

Dorsey does not disclose the use of a multi-stage, multi-dimensional finite state machine.

However, Nackman discloses the use of a multi dimensional finite state machine (column 9, lines 4-7).

Dorsey and Nackman do not disclose

the use of a multi-stage machine.

However, Sternberg discloses

the use of a multi-stage machine (column 3, lines 53-54).

The motivation of this claim is as same as the one of claim 12 above.

27. As to claim 26, Dorsey discloses an apparatus, comprising:

a logic unit (Fig.2, controller 24, column 5, line 11) configured to implement a message converter (column 5, lines 11-13) having a first finite state machine (Fig.5, a microcoded, pipeline control unit 59, column 7, line 14) that performs data format and

protocol conversion on an input message to produce an output message (column 5, lines 7-9; column 7, lines 14-16). Dorsey does not disclose the first finite state machine is multi-stage, multi-dimensional state machine.

However, Nackman discloses the first finite state machine is multi-dimensional state machine (column 9, lines 4-7).

Dorsey and Nackman do not disclose

the first finite state machine is multi-stage machine

However, Sternberg discloses the first finite state machine is multi-stage machine (column 3, lines 53-54).

The motivation of this claim is as same as the one of claim 12 above.

30. As to claim 30, Dorsey discloses the logic unit is further configured to recognize a communication protocol and a data format associated with the input message (column 4, lines 45-49), wherein the input message received from another apparatus (column 4, line 45, i.e., a package is received from network inter face 20a implying message is received for another apparatus).

28. As to claim 31, Dorsey discloses an apparatus, comprising:

an input/output unit (Fig.2, network interface 20a/20b embedded in network cards, column 4, lines 20-22) configured to perform communication with devices external to the apparatus (column 4, lines 20-25).

first means (Fig.2, the multi-protocol translator 26 and the direct memory access controller 27, column 5, lines 23-25) for performing protocol and data format translation on an input message to produce an output message (column 5, lines 25-28).

29. As to claim 32 Dorsey discloses the apparatus is a portable wireless device (it would have been obvious to the one skill in the art at the time of the invention to embed the translator 28 in Fig.2 into a portable wireless device), and wherein the first means includes a reprogrammable memory (column 6, lines 64-67).

30. As to claim 34 Dorsey discloses One or more computer readable media storing program instructions executable by a computing device to implement for converting an input message to an output message (column 5, lines 25-27), including converting a first communication protocol of the input message to a second communication protocol for the output message (column 5, lines 25-27, i.e., translating the header and trailer from the first protocol into the header and trailer information or a new packet meaning translating the first communication protocol to the second communication protocol; column 9, lines 43-45), and further including converting a first data format of the input message to a second data format of the output message (column 10, lines 2-3). Dorsey does not disclose a multi-stage, multi-dimensional finite state machine. However, Nackman discloses a multi-dimensional finite state machine (column 9, line 4-7). Dorsey and Nackman do not disclose a multi-stage machine. However, Sternberg discloses a multi-stage machine (column 3, lines 53-54).

The motivation of this claim is as same as the one of claim 12 above.

31. Claims 15-17, 22, 23, 29, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Nackman, in view of Sternberg as applied to claim 12 above, in view of Netravali et al. (hereinafter Netravali), U.S Patent No. 5680552.

32. As to claims 15, 23, 29 and 36 Dorsey, Nackman and Sternberg disclose the invention as described in claims 12, 20, 26 above. Dorsey further discloses one or more of the following inputs: 1) inputs indicative of a) the type of source application that originated the input message (column 12, lines 8-12), and b) the type of destination application to which the output message is directed (column 10, lines 2-3, column 12, lines 8-12);

Dorsey does not disclose 2) inputs indicative of a) the type of a first device from which the input message originated and b) the type of a second device to which the output message is directed; 3) input indicative of a current connection status between the first and second devices, and 4) input indicative of the current state of the finite state machine.

However, Netravali discloses 2) inputs indicative of a) the type of a first device from which the input message originated (column 4, lines 4-10) and b) the type of a second device to which the output message is directed (column 4, lines 4-10); 3) input indicative of a current connection status between the first and second devices (column

8, lines 29-41), and 4) input indicative of the current state of the finite state machine (column 5, lines 63-65; column 6, lines 3-5).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Nackman and Sternberg with the teaching of Netravali to have 2) inputs indicative of a) the type of a first device from which the input message originated and b) the type of a second device to which the output message is directed; 3) input indicative of a current connection status between the first and second devices, and 4) input indicative of the current state of the finite state machine. Because it would provide users a better, simple and efficient method to construct protocol converters by using circuits that perform the operations of the set of protocol finite state machines for the protocols, the first and the second complement network protocol finite state machine, as well as interface converters.

33. As to claims 16, 17, and 33 Dorsey, Nackman and Sternberg disclose the invention as described in claims 12, 31 above, Dorsey, Nackman and Sternberg do not disclose inputs to one or more stages of the finite state machine include one or more reserved inputs, the method further comprising using at least one of the reserved inputs to update the operation of the finite state machine. However, Netravali discloses inputs to one or more stages of the finite state machine include one or more reserved inputs (column 14, lines 54-56), the method further comprising using at least one of the reserved inputs to update the operation of the finite state machine (column 11, lines 59-65).

The motivation of these claims is as same as the one of claim 15 above.

34. As to claim 22, Dorsey, Nackman, and Sternberg disclose the invention as described in claim 20 above. Dorsey discloses the use of reprogramming of the memory (column 6, lines 64-67). Dorsey, Nackman, and Sternberg do not disclose the finite state machine includes one or more reserved inputs, and wherein the reserved inputs are usable, via reprogramming of the memory, to update operation of the finite state machine to accommodate a future communication protocol and/or data format. However, Netravali discloses the finite state machine includes one or more reserved inputs, and wherein the reserved inputs are usable (column 14, lines 54-56), to update operation of the finite state machine to accommodate a future communication protocol and/or data format (column 11, lines 59-65).

The motivation of this claim is as same as the one of claim 15 above.

35. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Nackman, in view of Sternberg as applied to claim 12 above, further in view of Tiemann et al. (hereinafter Tiemann), U.S Patent No. 4903026.

36. As to claim 18, Dorsey, Nackman, and Sternberg disclose the invention as described in claim 12 above. Dorsey, Nackman and Sternberg do not disclose the one or more additional stages include a final stage having an output specifying 1) a current action to be taken in order to generated the output message, and 2) a next state of said

finite state machine. However, Tiemann discloses the one or more additional stages include a final stage (column 6, line 39) having an output specifying 1) a current action to be taken in order to generated the output message (column 6, lines 38-41), and 2) a next state of said finite state machine (column 6, lines 54-57).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Nackman, and Sternberg with the teaching of Tiemann to have the one or more additional stages include a final stage having an output specifying 1) a current action to be taken in order to generated the output message, and 2) a next state of said finite state machine. Because it would provide users a better architecture for implementing high resolution from analog to digital converters that operate at high sampling rate, a better A/D converter system with a self-calibration capability which is effective even during noisy signal input, allowing for selective calibration under external control (column 2, lines 1-10).

37. Claims 21, 25, 27, 28, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Nackman, in view of Sternberg as applied to claim 20 above, further in view of O' Hagan et al. (hereinafter O'Hagan), U.S Patent No. 6424830.

38. As to claims 21 and 27, Dorsey, Nackman, and Sternberg disclose the invention as described in claims 20 and 26 above. Dorsey discloses at least a portion of the memory is reprogrammable (column 6, lines 64-67) to update operation of the finite state machine (column 9, lines 5-7, fed means update).

Dorsey, Nakman and Sternberg do not disclose the input message originates from the apparatus, and wherein the apparatus is configured to convey the output message to a separate apparatus. However, O'Hagan discloses the input message originates from the apparatus (column 4, lines 41-44), and wherein the apparatus is configured to convey the output message to a separate apparatus (column 4, lines 41-44).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Nackman, and Sternberg with the teaching of O'Hagan to have the input message originates from the apparatus, and wherein the apparatus is configured to convey the output message to a separate apparatus. Because it would provide user a better method to utilize the RF transceiver being configured to communicate information in packets in accordance with a carrier sense multiple access (CSMA) protocol; a speaker; and a control circuit, operatively coupled to the input means, the RF transceiver, and the speaker, for selectively enabling the RF transceiver to transmit data based on data input via the input means and to convert voice data received by the RF transceiver into a voice signal which is output through the speaker (column 3, lines 14-22).

39. As to claim 25, Dorsey, Nackman, and Sternberg disclose the invention as described in claims 20 and 21 above. They do not disclose the apparatus is a portable wireless device, and wherein the input message originates from a separate apparatus. However, O'Hagan discloses the apparatus is a portable wireless device (column 4, line

19), and wherein the input message originates from a separate apparatus (column4, lines 41-44).

The motivation of this claim is as same as the one of claim 21 above.

40. As to claim 28, Dorsey, Nackman and Sternberg disclose the invention as described in claim 26 above. Dorsey further discloses the logic unit is an ASIC (column 5, lines 11-13). Dorsey, Nackman and Sternberg do not disclose the apparatus is a portable device, wherein the apparatus is configured to use the message converter to communicate with a plurality of devices that do not have a corresponding message converter. However, O'Hagan discloses the apparatus is a portable device (column 4, line 19), wherein the apparatus is configured to use the message converter to communicate with a plurality of devices that do not have a corresponding message converter (column 4, lines 35-40).

The motivation of this claim is as same as the one of claim 21 above.

41. As to claim 35, Dorsey, Nackman and Sternberg disclose the invention as described in claim 34 above, they do not disclose the media stores program instructions executable by the computing device to receive the input message wirelessly or transmit the output message wirelessly. However, O'Hagan discloses the media stores program instructions executable by the computing device to receive the input message wirelessly or transmit the output message wirelessly (column 6, lines 64-67; column 7, lines 1-4, 10-12).

The motivation of this claim is as same as the one of claim 21 above.

42. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey, Nackman, Sternberg as applied to claim 20 above, in view of Broulik, and further in view of Thomas J. Campana, Jr. (hereinafter Campana, Jr.), U.S Patent No. 5694428.

43. As to claim 24, Dorsey, Nackman, and Sternberg disclose the invention as described in claim 20 above. They do not disclose a message router coupled to receive the output message, and configured to determine one of the plurality of sender units to send the output message according to a desired communication protocol for the output message. However, Broulik discloses a message router coupled to receive the output message (Fig.2, proxy 26) and configured to determine the sender unit to send the output message according to a desired communication protocol for the output message (column 4, lines 32-39).

Broulink does not disclose a plurality of sender units configured to transmit the output message. However, Campana, Jr. discloses a plurality of sender (Fig.7 a plurality of transmitters 124, column 39, line 5) units configured to transmit the output message (column 39, lines 5-8).

It would have been obvious to the one skilled in the art at the time of the invention to combine the teaching of Dorsey, Nackman, Sternberg, and Broulik with the teaching of Campana, Jr. to have a message router coupled to receive the output message, and configured to determine one of the plurality of sender units to send the

output message according to a desired communication protocol for the output message. Because it would provide users a better way of load-balancing for sending messages to destination devices, transmitting package data to destination devices by using deferent protocols.

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Siegel et al.	US 5073852
Heimendinger et al	US 6278532
Shawn Thomas Segur	US 6212550
Leslie et al.	US 6404775
Cline et al.	US 5655001

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BANGLONG TRAN whose telephone number is (571)270-3931. The examiner can normally be reached on Monday-Friday 8:00 a.m.-5:00p.m, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton B. Burgess can be reached on (571)272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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